

Amendments to the Claims

1. *(Currently Amended)* Reset circuit (1) comprising a clock signal input (~~RC~~) for receiving a clock signal (~~CL~~) consisting of a sequence of clock signal cycles, comprising a data signal input (~~RD~~) for receiving digital data signals (~~MD~~), said digital data signals (~~MD~~) being encoded in such a manner that at least one signal edge (~~0~~ → 1, 1 → 0) appears per data bit in the data signal, comprising a counting stage (2) being connected to the data signal input (~~RD~~) and the clock signal input (~~RC~~) and being designed for counting a number (~~X~~) of clock signal cycles, which clock signal cycles appear between a defined number of data signal edges, and comprising comparing means (3), said comparing means (3) being designed for comparing the number (~~X~~) of clock signal cycles counted by the counting stage (2) with a lower limit (~~MIN~~) and/or with an upper limit (~~MAX~~) and said comparing means (3) being designed to emit a reset signal (~~RS~~), if the number (~~X~~) either remains below the lower limit (~~MIN~~) or exceeds the upper limit (~~MAX~~), depending on the limit value (~~MIN~~, ~~MAX~~) taken for comparison.

2. *(Currently Amended)* A data carrier (4, 4') comprising a logic circuit (5), said logic circuit (5) being designed for receiving digital data signals (~~MD~~) and for producing output data (~~AD~~) and for receiving a reset signal (~~RS~~), said reset signal (~~RS~~) being provided to set the logic circuit (5) into a defined logical state, wherein the data carrier (4, 4') comprising a reset circuit (1) as claimed in claim 1 and wherein the reset signal (~~RS~~) of the reset circuit (1) being provided to be supplied to the logic circuit (5).

3. *(Currently Amended)* A data carrier (4, 4') as claimed in claim 2, wherein the data carrier (4, 4') comprising a pad (6) for connecting external data input lines, data output lines, clock signal lines and preferably power supply lines to the reset circuit (1) and the logic circuit (5), respectively.

4. *(Currently Amended)* A data carrier (4, 4') as claimed in claim 2, wherein the data carrier (4) comprising a coupling element (7) for contactless transmission of signals and comprising an air interface (8) for processing received signals, wherein

the air interface (8) being provided for extracting data signals (MD) and clock signals (CL) from the received signals and for forwarding the extracted data signals (MD) to the reset circuit (1) and the logic circuit (5), respectively.

5. *(Currently Amended)* A data carrier (4,4') as claimed in claim 4, wherein the air interface (8) being designed for extracting electrical energy for supplying the reset circuit (1) and the logic circuit (5) with energy, wherein the extracted electrical energy being preferably buffered intermediately in an energy storage means (9).

6. *(Currently Amended)* A data carrier (4,4') as claimed in claim 2, wherein the data carrier (4') comprising a subscriber's identification module (SIM) for a mobile telephone application.

7. *(Currently Amended)* A communication device (10), comprising a data carrier (4,4') as claimed in ~~any one of the claims 2 to 6~~ claim 2.

8. *(Currently Amended)* A communication device (10), being designed for communicating with a data carrier (4,4') as claimed in ~~any one of the claims 3 to 6~~ claim 3, wherein the communication device (10) comprising a coupling element (7') for contactless transmission of signals and an air interface (8') for processing received signals, wherein the air interface (8') being provided for extracting digital data reception signals (MD) and clock signals (CL) from the received signals and for making the digital data reception signals available for forwarding to the data carrier (4,4').

9. *(Currently Amended)* A communication device (10) as claimed in claim 8, wherein the air interface (8') comprising a pseudo data generator (11), said data generator (11) being designed for making a pseudo data signal, which said pseudo data signal being coded in such a way that at least one signal edge occurs per data bit in the data signal, available for forwarding to the data carrier, if no signals can be received by the coupling element (7'), from which signals valid data reception signals (MD) could be extracted.

10. *(Currently Amended)* A communication device ~~(10)~~ as claimed in claim 8, wherein the air interface ~~(8')~~ comprising a pseudo clock signal generator ~~(12)~~, said pseudo clock signal generator ~~(12)~~ being designed for making available a pseudo clock signal consisting of a sequence of clock signal cycles for forwarding to the data carrier, if no electromagnetic signals can be received by the coupling element ~~(7')~~, from which electromagnetic signals valid clock signals ~~(CL)~~ could be extracted.

11. *(Currently Amended)* A communication device ~~(10)~~ as claimed in ~~any one of the claims 7 to 10~~ claim 7, wherein the communication device ~~(10)~~ being designed as a mobile phone, a personal digital assistant (~~PDA~~) or a personal computer.

12. *(Currently Amended)* A reset method for resetting a data carrier ~~(4, 4')~~ and its logic circuit ~~(5)~~, respectively, in a defined logical state, comprising reception of a clock signal ~~(CL)~~ consisting of a sequence of clock signal cycles, and comprising reception of digital data signals ~~(MD)~~, said digital data signals ~~(MD)~~ being encoded in such a manner that at least one signal edge appears per data bit in the data signal ~~(MD)~~, and comprising counting of a number ~~(X)~~ of clock signal cycles, which clock signal cycles appear between a defined number of data signal edges, and comprising comparison of the number ~~(X)~~ of counted clock signal cycles with a lower limit ~~(MIN)~~ and / or with an upper limit ~~(MAX)~~ and comprising emitting of a reset signal ~~(RS)~~ for the logic circuit ~~(5)~~, if the number ~~(X)~~ either remains below the lower limit ~~(MIN)~~ or exceeds the upper limit ~~(MAX)~~, depending on the limit value ~~(MIN, MAX)~~ taken for comparison.